Design of an Integrated Image Sensor System

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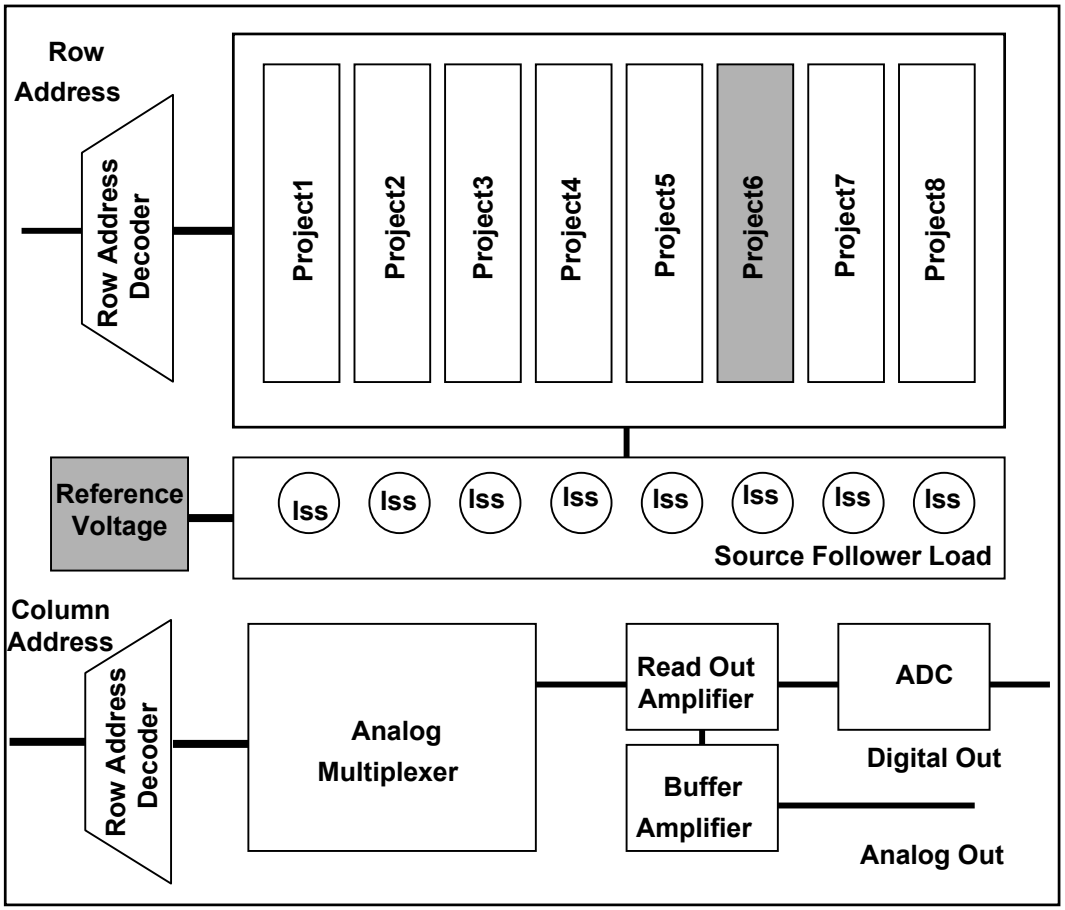
Design Goals

- **Individual Task:**

  Design a APS row sensor with shutter arrangement

- **Global Task:**

  Design a biasing current supply circuit



Overview

1. APS Row Sensor Design

1.1 Characteristics of CMOS Image Sensor Design

1.1.1 Configuration

1.1.2 Responsibility

1.1.3 Transfer Function

1.1.4 Output Performance

1.1.5 schematic design

1.2 Layout Drawing and simulation

1.3 Results

2. Biasing Current Circuit Design

2.1Application

2.2 Formulas

2.3 Design Parameters

2.4 raw schematic

APS Row Sensor Design

1.1 Characteristics of APS Row Sensor Design

1.1.1 Configuration

- Resolution: 0.35um-4-metal COMS Technology
  --Austria Microsystems Technology
- Photo Detector type : N-diffusion Photodiode
- Fill Factor : Photosensitive Area / Pixel Area
- Array Size : 4*16 pixels

APS Row Sensor Design

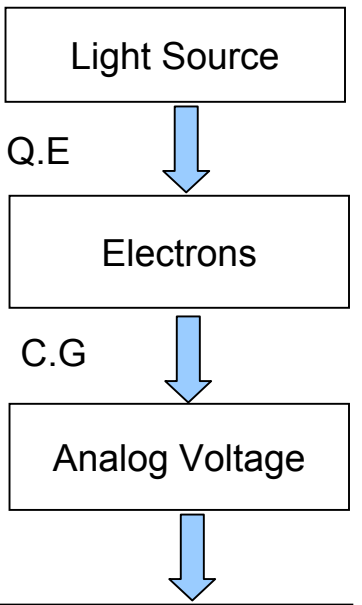
1.1.2 Responsibility

- Quantum efficiency: measurement of the device's electrical sensitivity to light

$$QE = \frac{\text{electrons/sec}}{\text{photons/sec}} = \frac{\text{current/(charge of 1 electron)}}{\text{(total power of photons)/(energy of one photon)}}$$

It depends on absorption and collection of charges

For simulation we set I_{photon} : 100pA~900pA



- Conversion Gain: transfer capability from the input electrons to the output voltage

C.G= Vout/Number of Electrons
= q/C(total)

APS Row Sensor Design

1.1.3 Transfer Function

- Dynamic Range: it quantifies the sensor's ability to adequately image both high lights and dark shadow in scene.

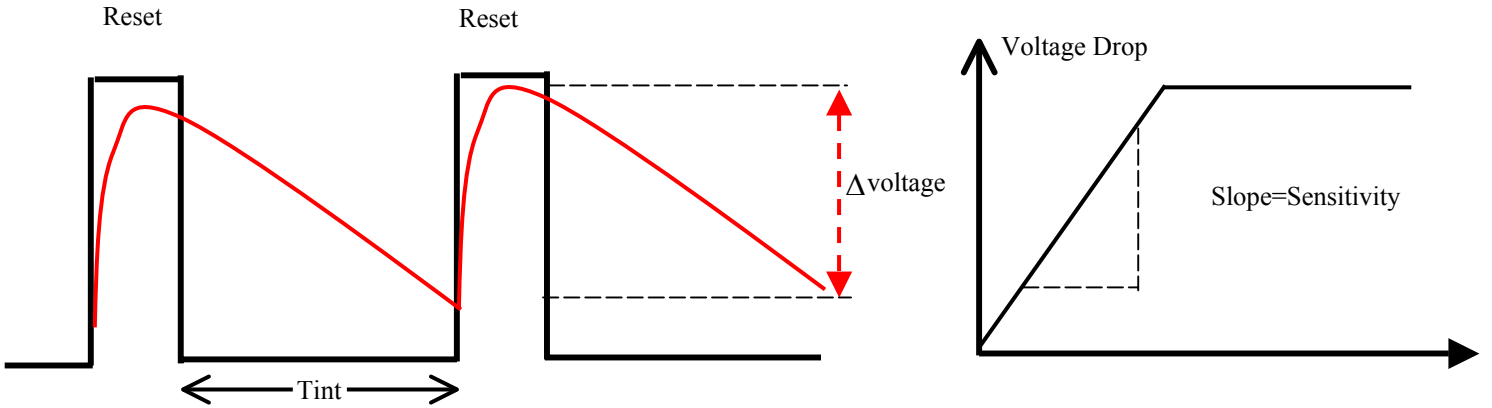
$$\mathrm{DR} = 20\log_{10}\frac{i_{max}}{i_{min}} = 20\log_{10}\frac{Q_{sat}}{\sqrt{qi_{dc}T + \sigma_V^2 + \sigma_C^2}}.$$

I max – the largest non –saturating photocurrent ⟸ Limited by well capacity Q sat

I min – the smallest detectable photocurrent ⟸ Limited by sensor read noise

APS Row Sensor Design

- Sensitivity : The ratio of voltage Response to the photo energy illumination

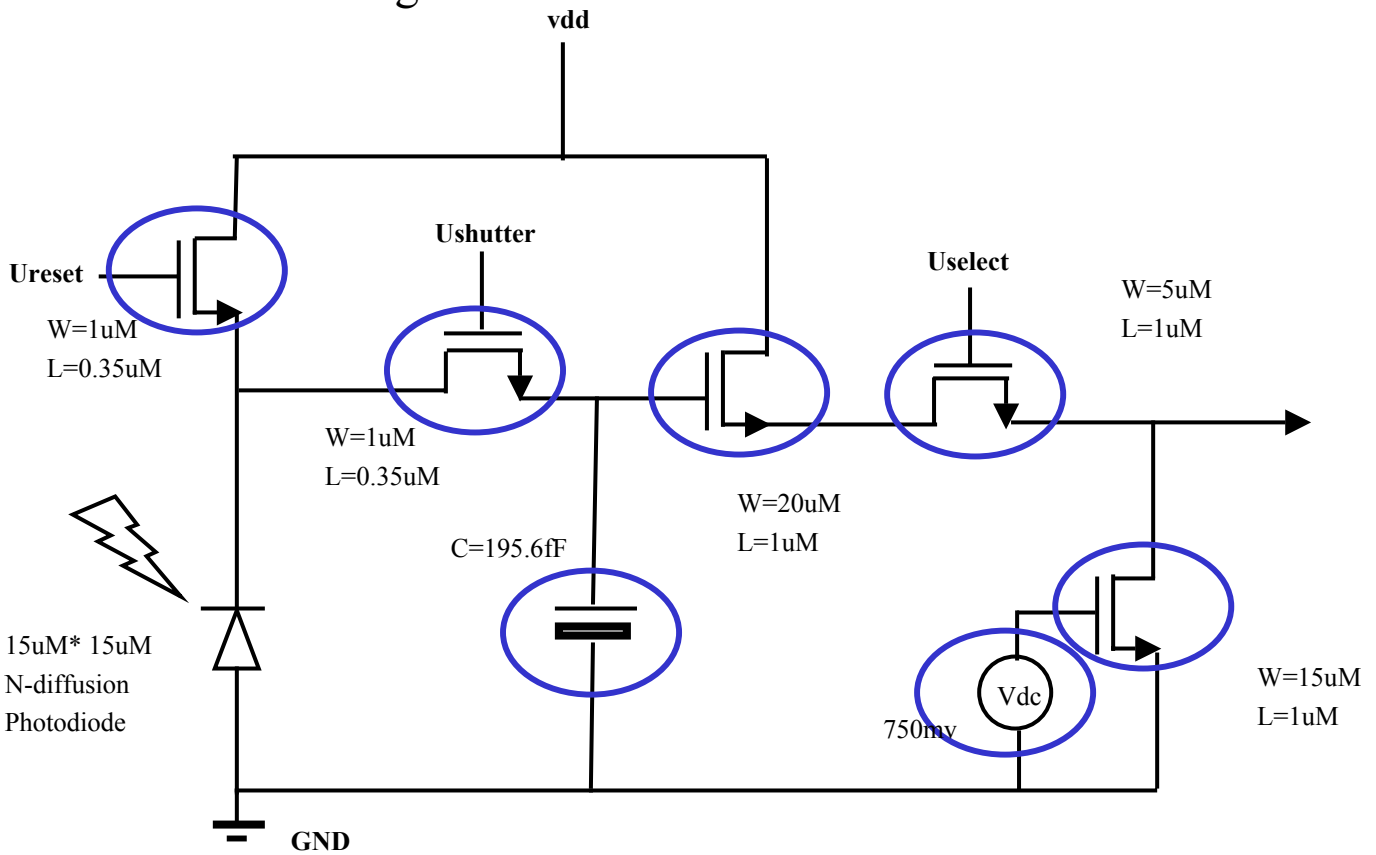


1.1.4 Output Performance

- Frame Rate—reverse proportional to Readout time
- Output Voltage

APS Row Sensor Design

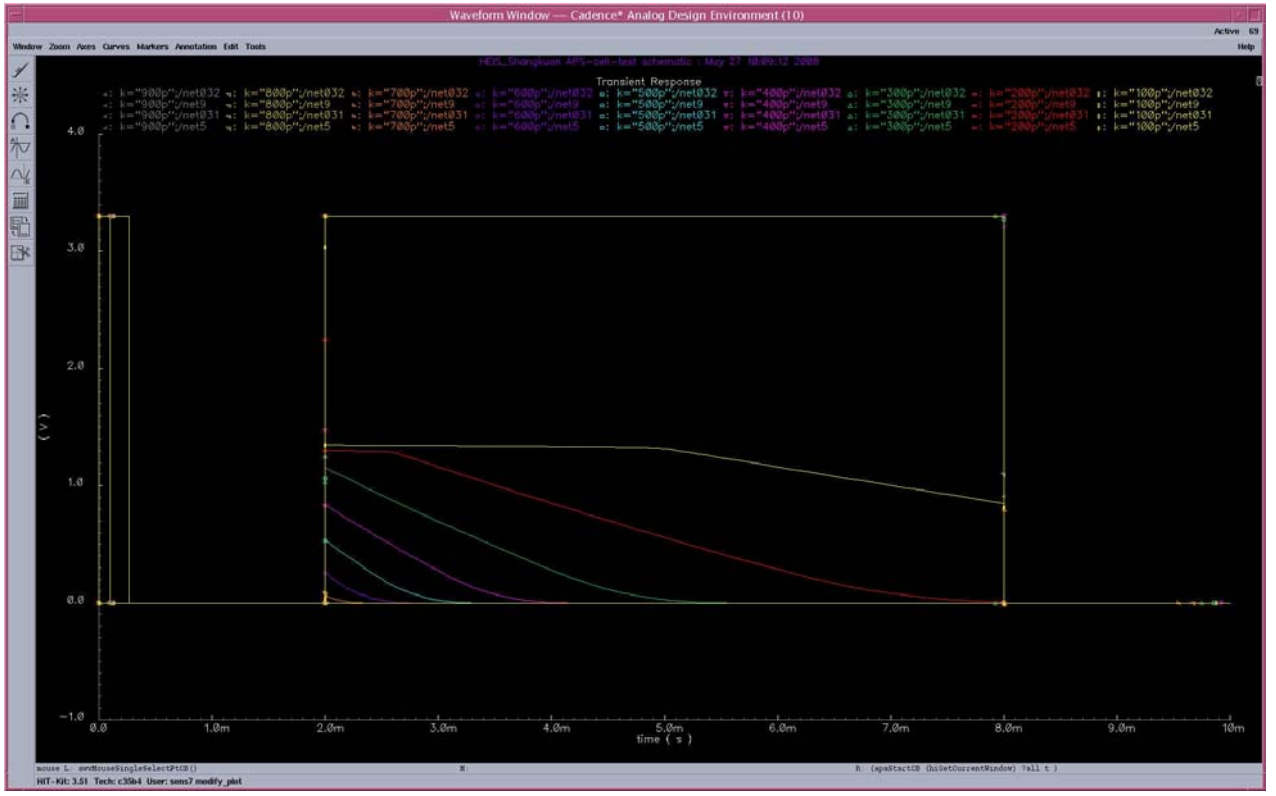
1.1.5 Schematic Design



APS Row Sensor Design

Single APS Cell Schematic-Shutter Arrangement

Simulated with Rest Signal (0.0V-3.3V,Pulse width 100uS,Delay Time 0S)



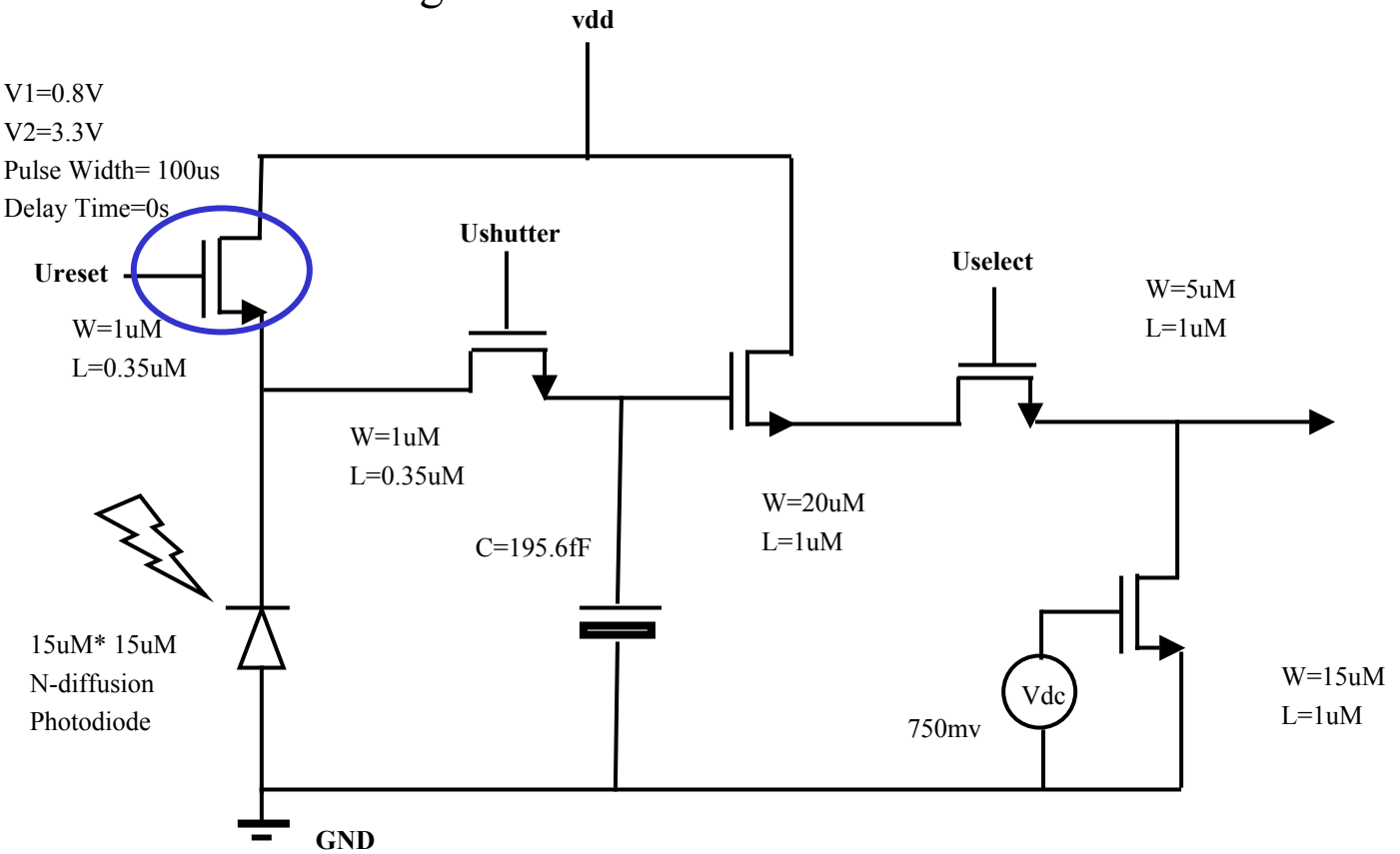
APS Row Sensor Design

Single APS Cell Schematic-Shutter Arrangement

Simulated with Rest Signal (0.8V-3.3V,Pulse width 100uS,Delay Time 0S)

APS Row Sensor Design

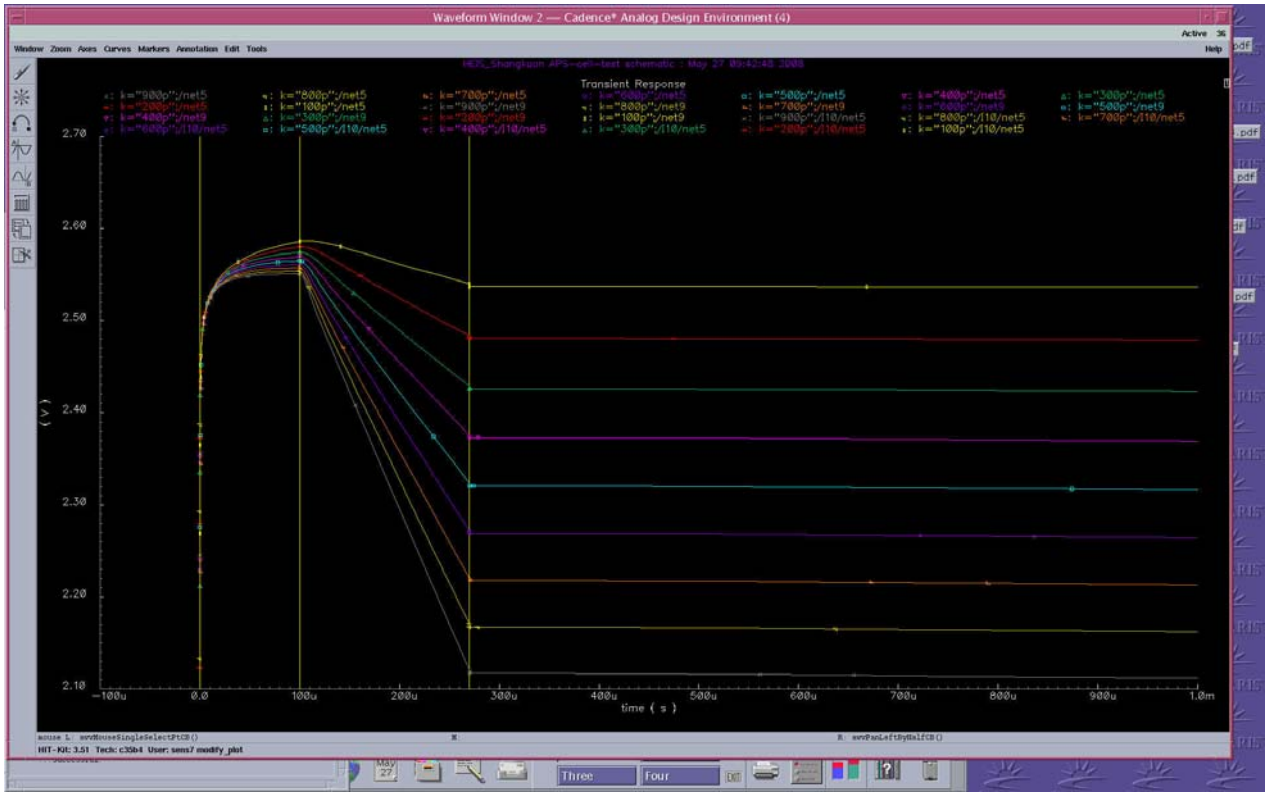
1.1.5 Schematic Design



APS Row Sensor Design

Single APS Cell Schematic-Shutter Arrangement

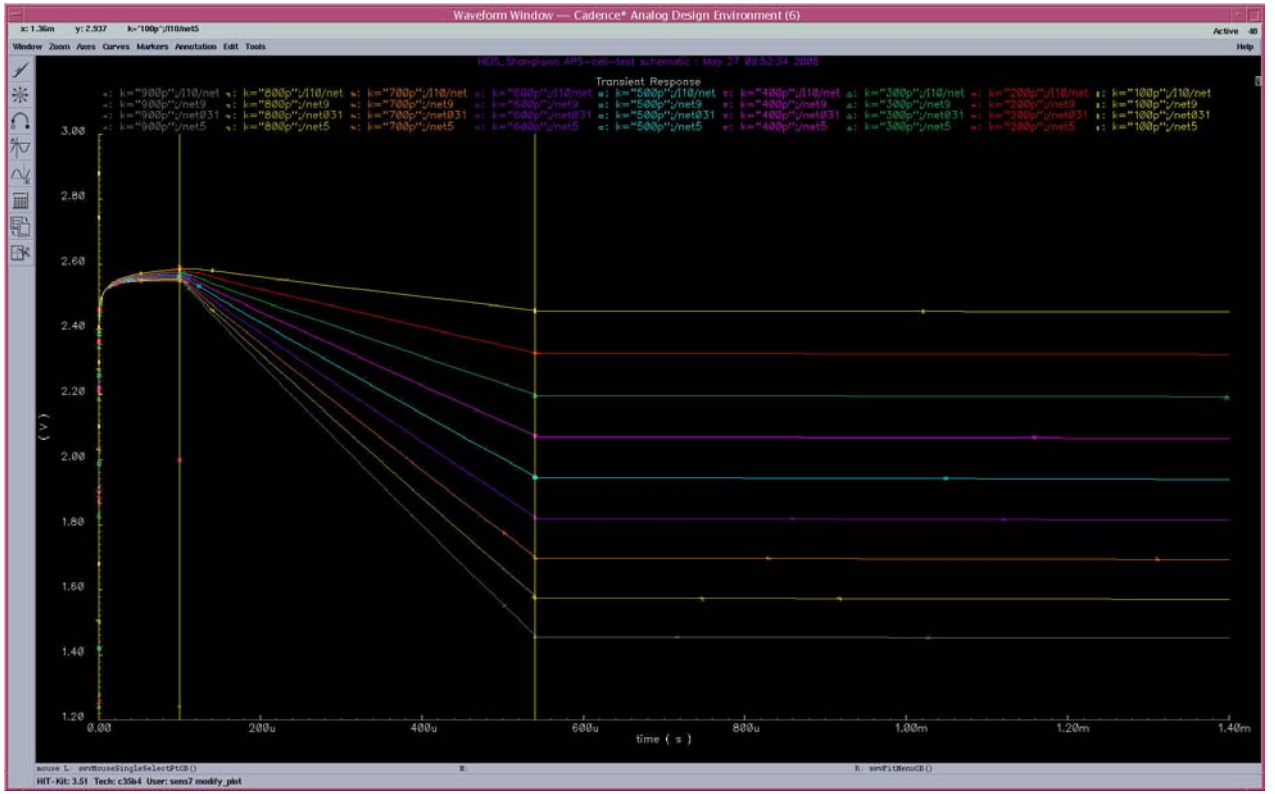
Simulated with Shutter Signal (0.0V-3.3V, Pulse width 270uS Delay Time 0 S)



APS Row Sensor Design

Single APS Cell Schematic-Shutter Arrangement

Simulated with Shutter Signal (0.0V-3.3V, Pulse width 540uS Delay Time 0 S)



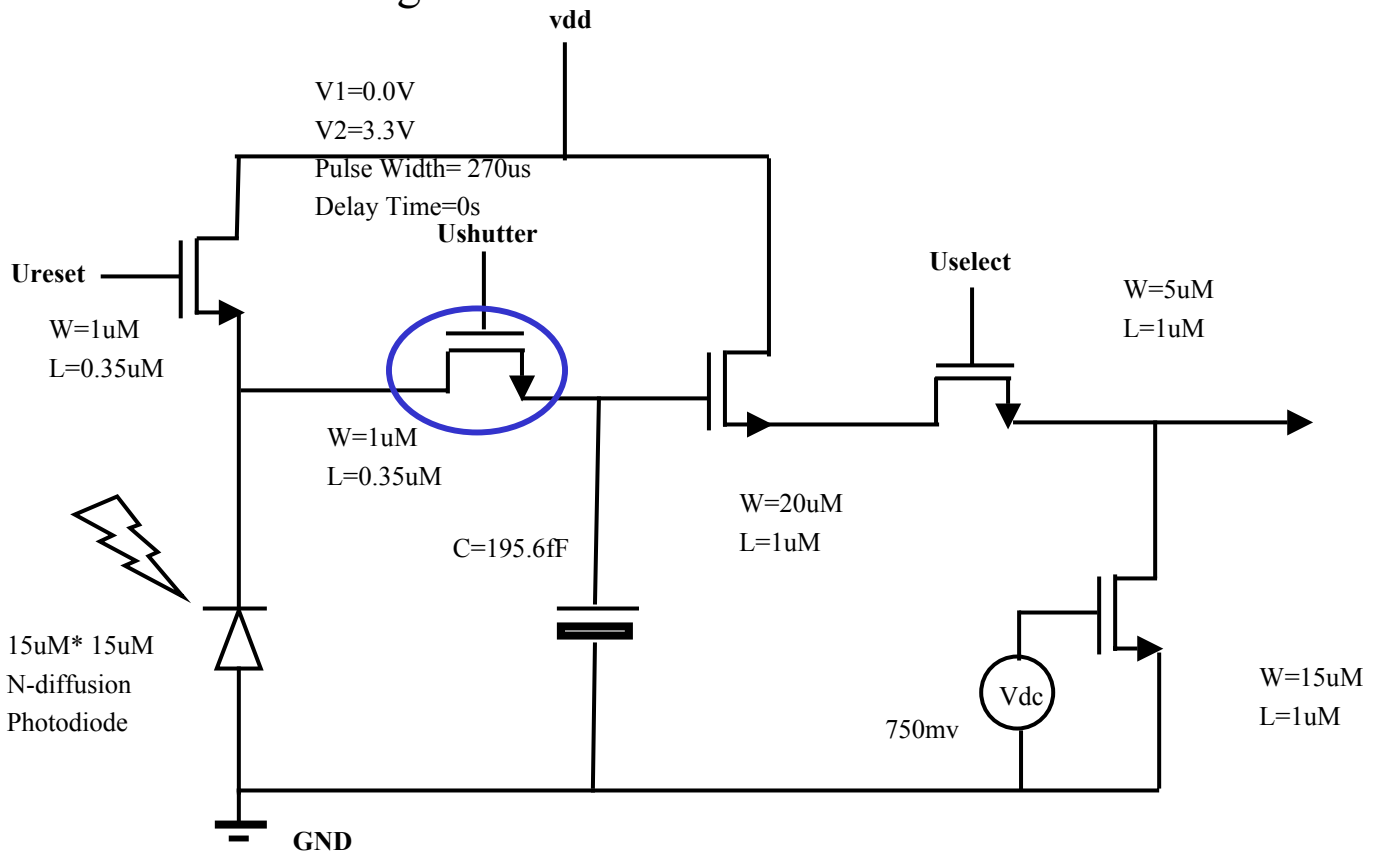
APS Row Sensor Design

Single APS Cell Schematic-Shutter Arrangement

$I_{photo(pA)}$	V_{cap}	V_{cap}
100	2.537	2.457
200	2.481	2.326
300	2.426	2.197
400	2.373	2.07
500	2.32	1.944
600	2.269	1.82
700	2.218	1.697
800	2.167	1.575
900	2.117	1.455
$\overline{\Delta v / \Delta Iphoto}$	0.0524V/100pA	0.126V/100pA

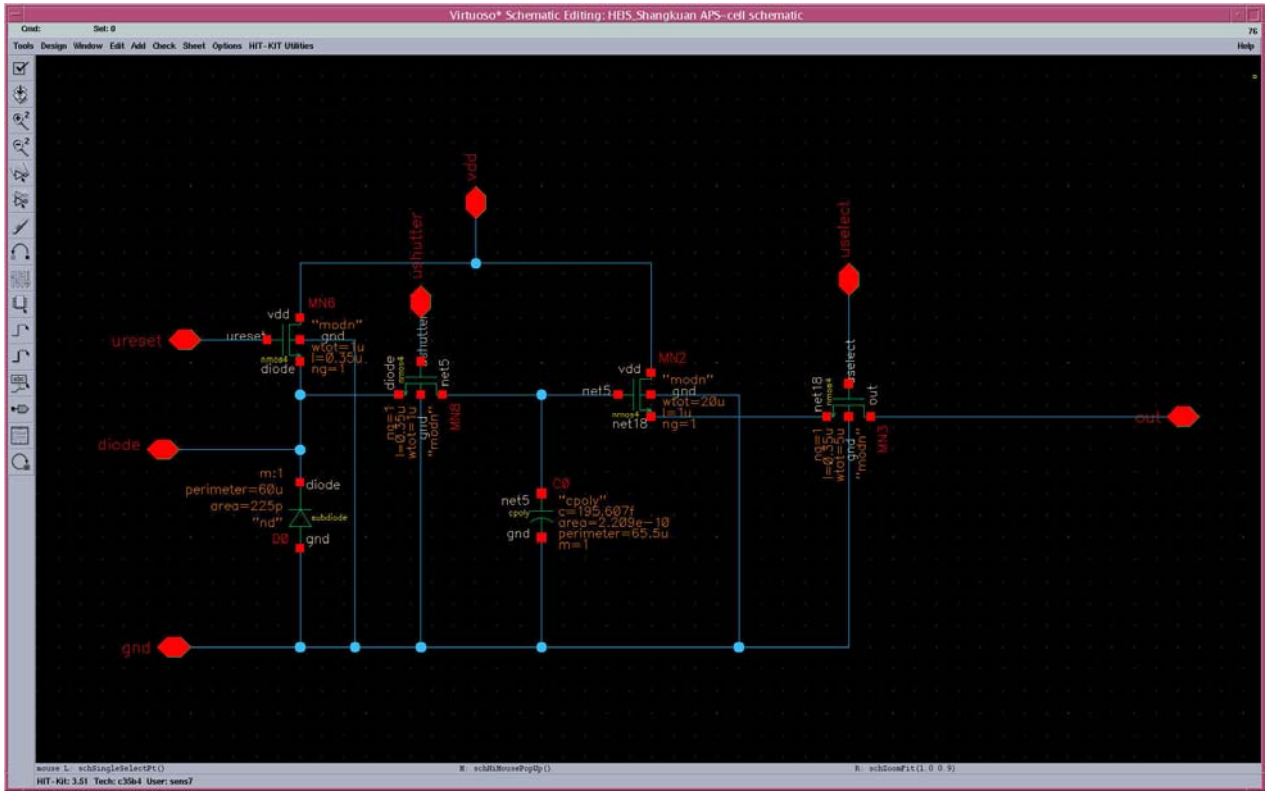
APS Row Sensor Design

1.1.5 Schematic Design



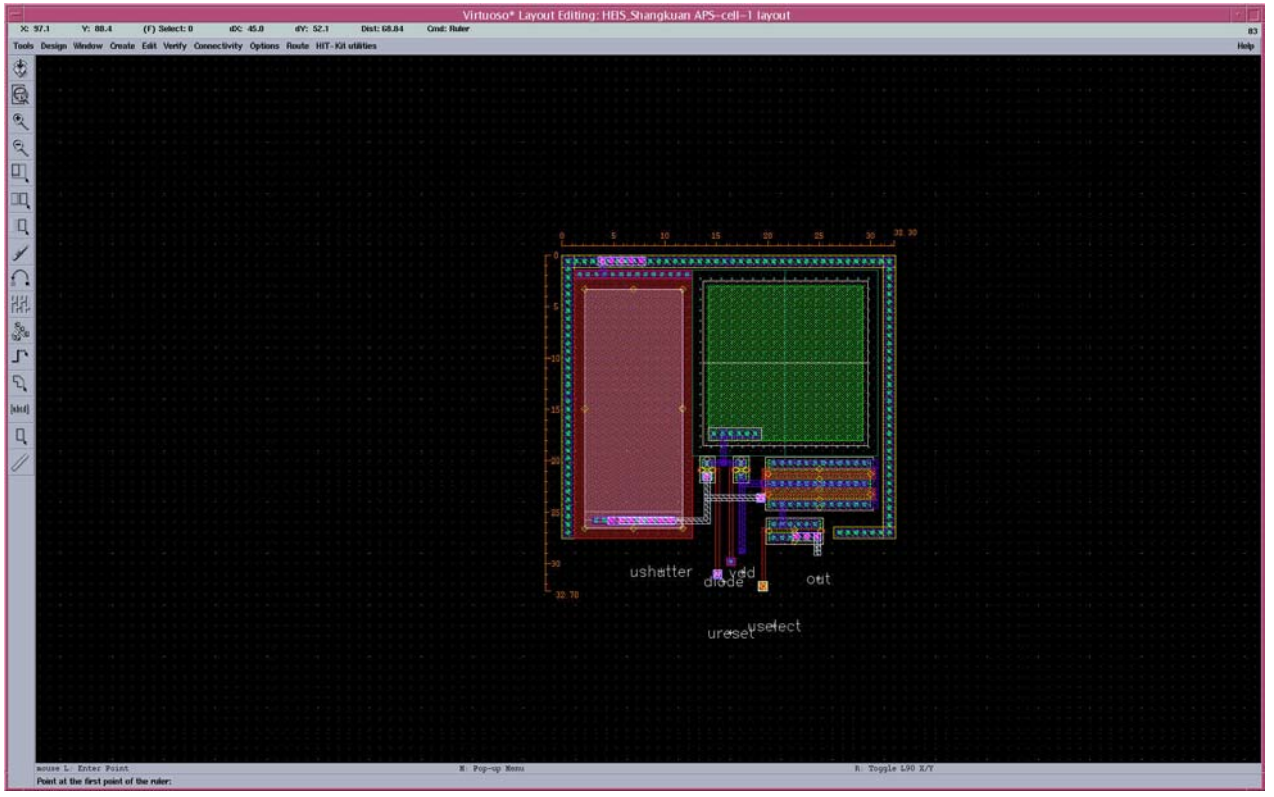
APS Row Sensor Design

Single APS Cell Schematic



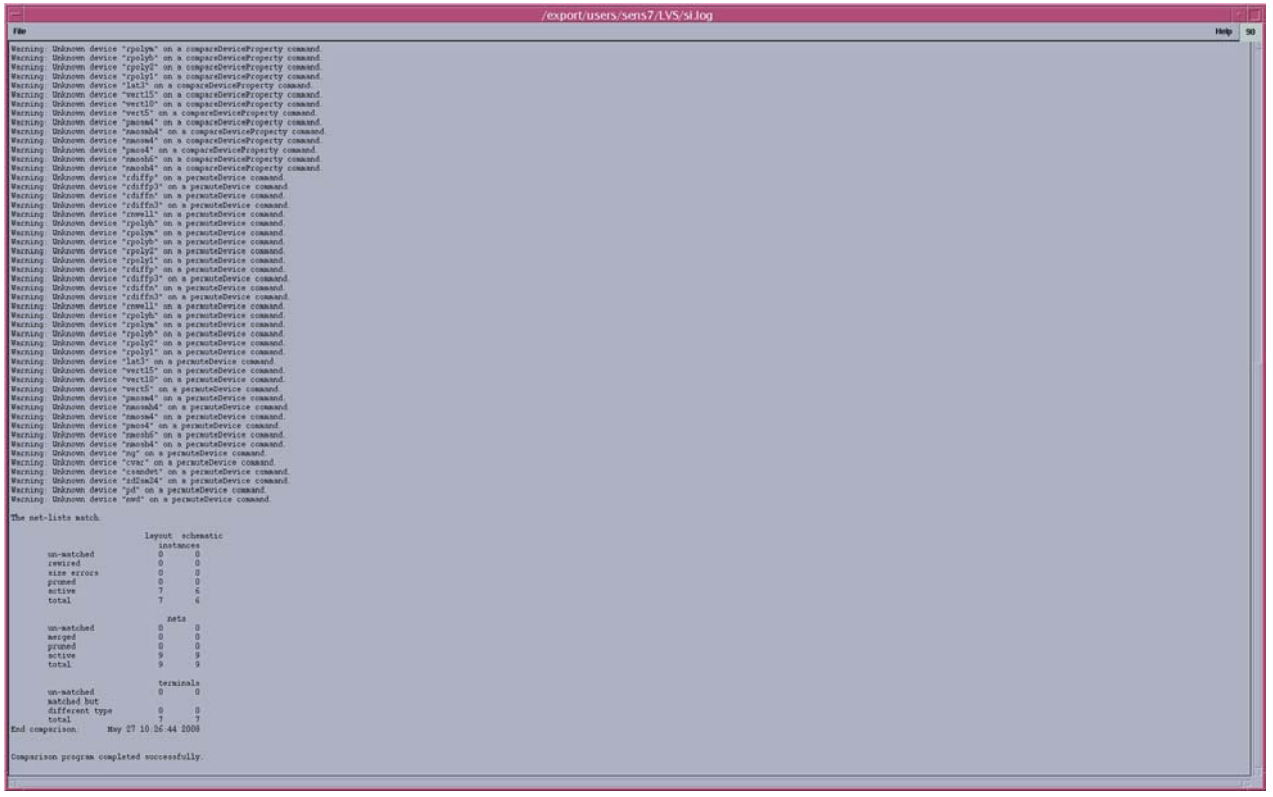
APS Row Sensor Design

Single APS Cell Layout



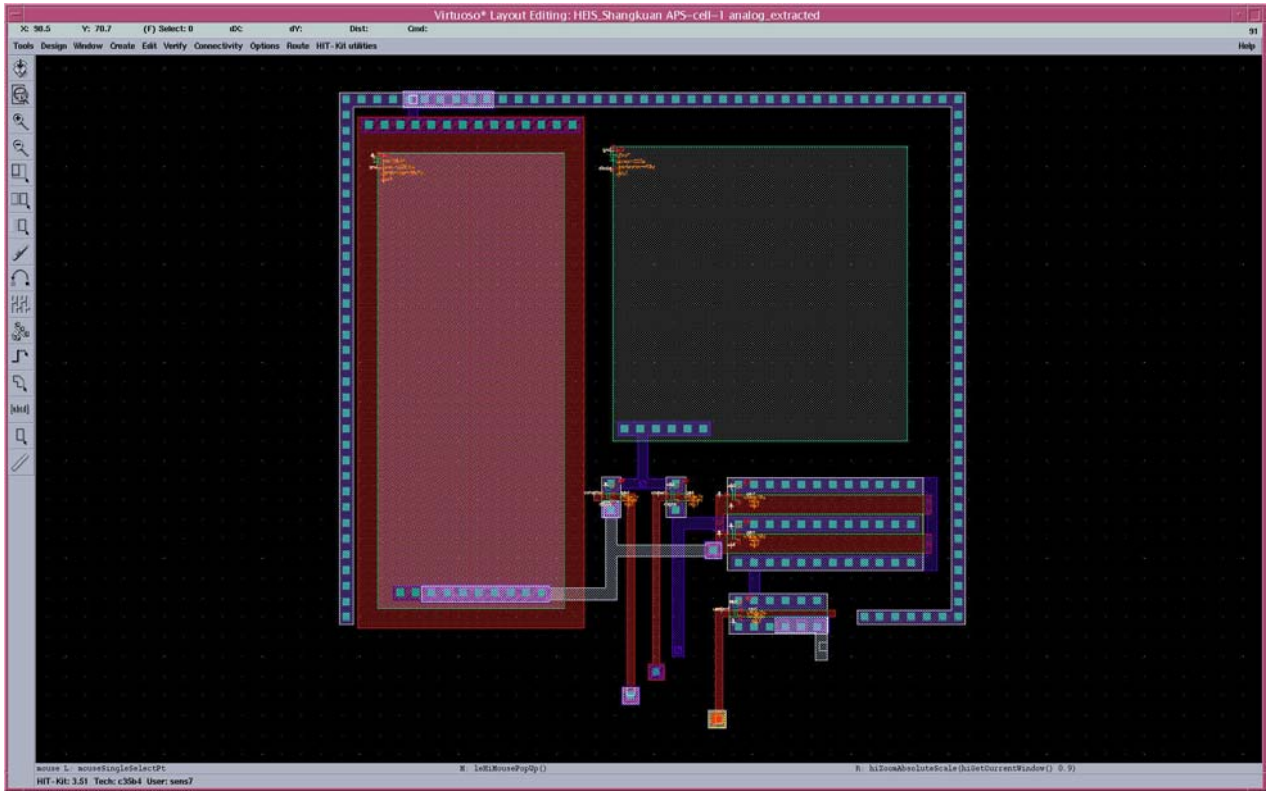
APS Row Sensor Design

Single APS Cell LVS Check



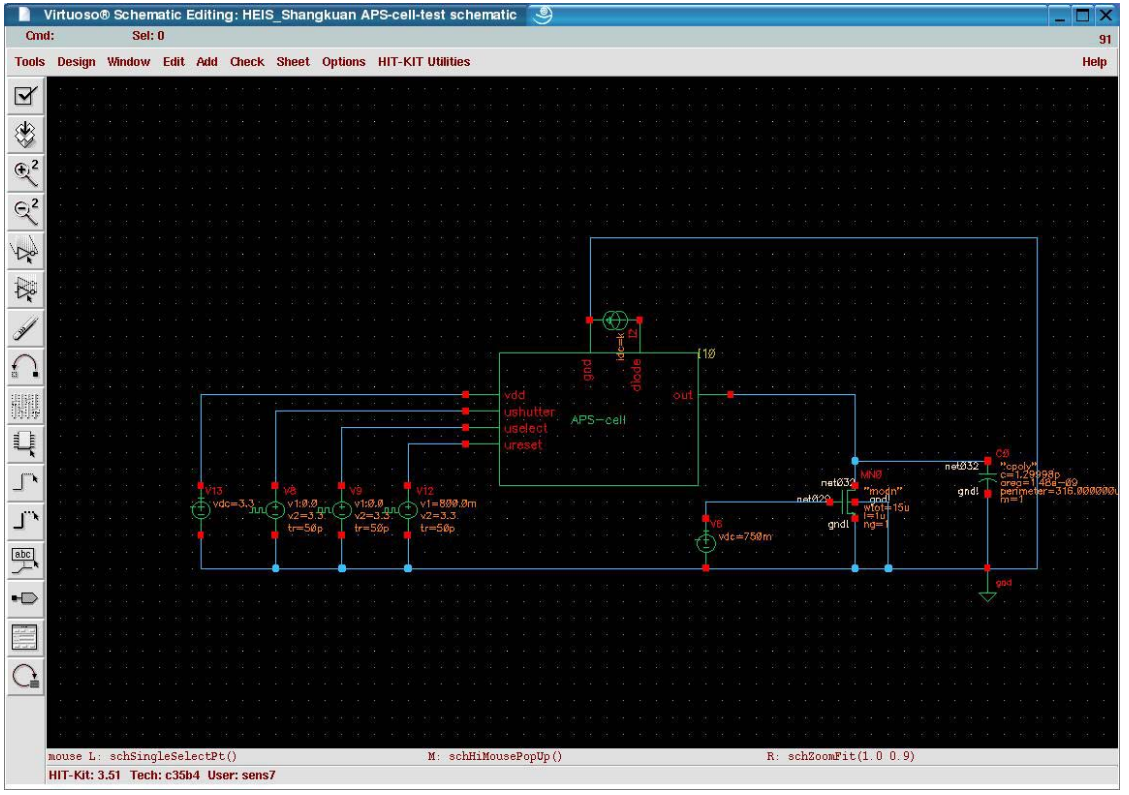
APS Row Sensor Design

Single APS Cell Analog-Extracted



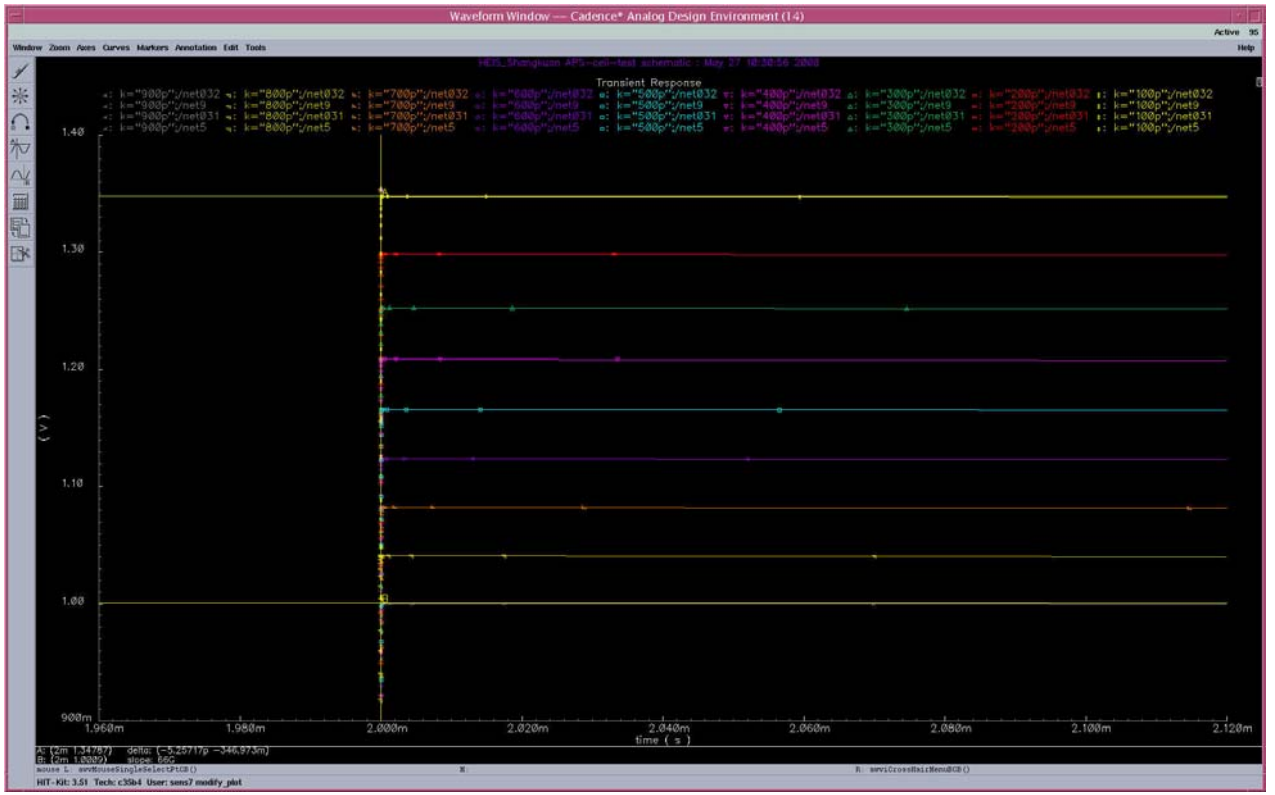
APS Row Sensor Design

Single APS Cell Test Schematic



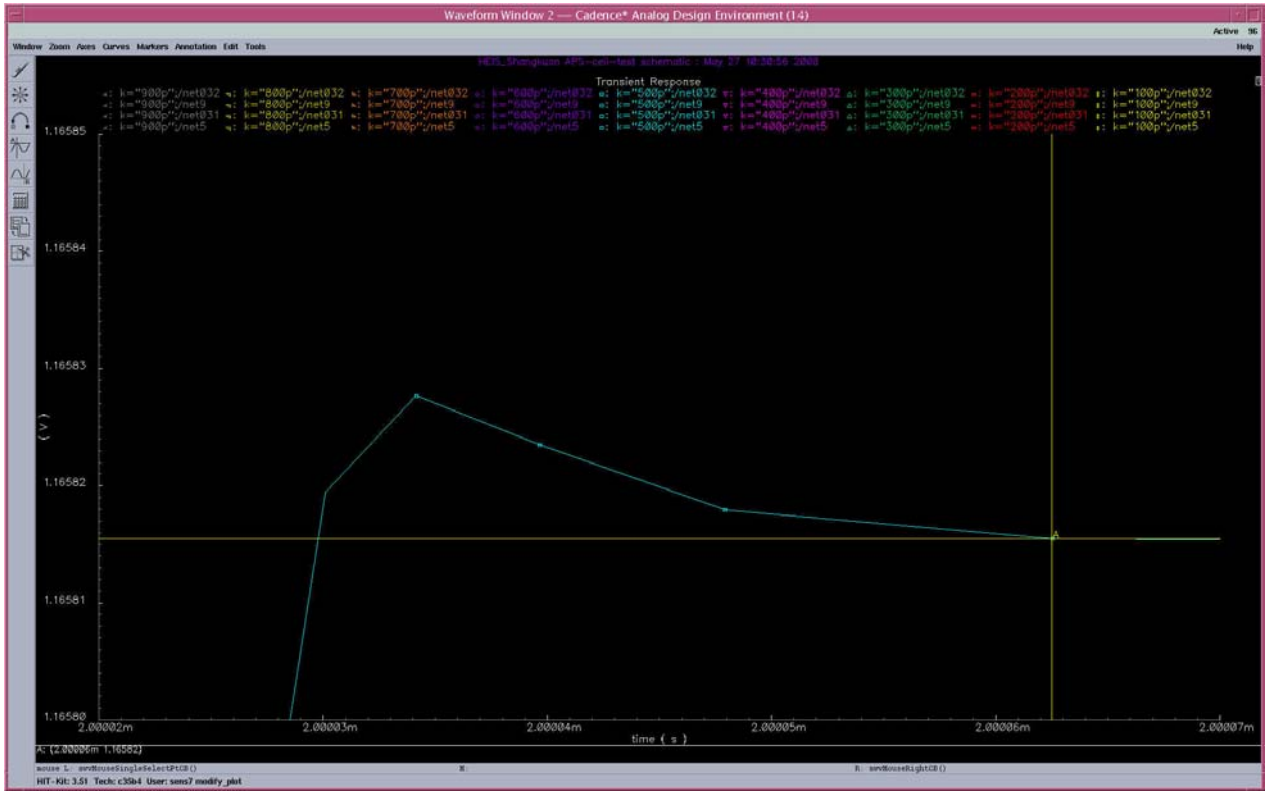
APS Row Sensor Design

Single APS cell Simulation-Output Voltage



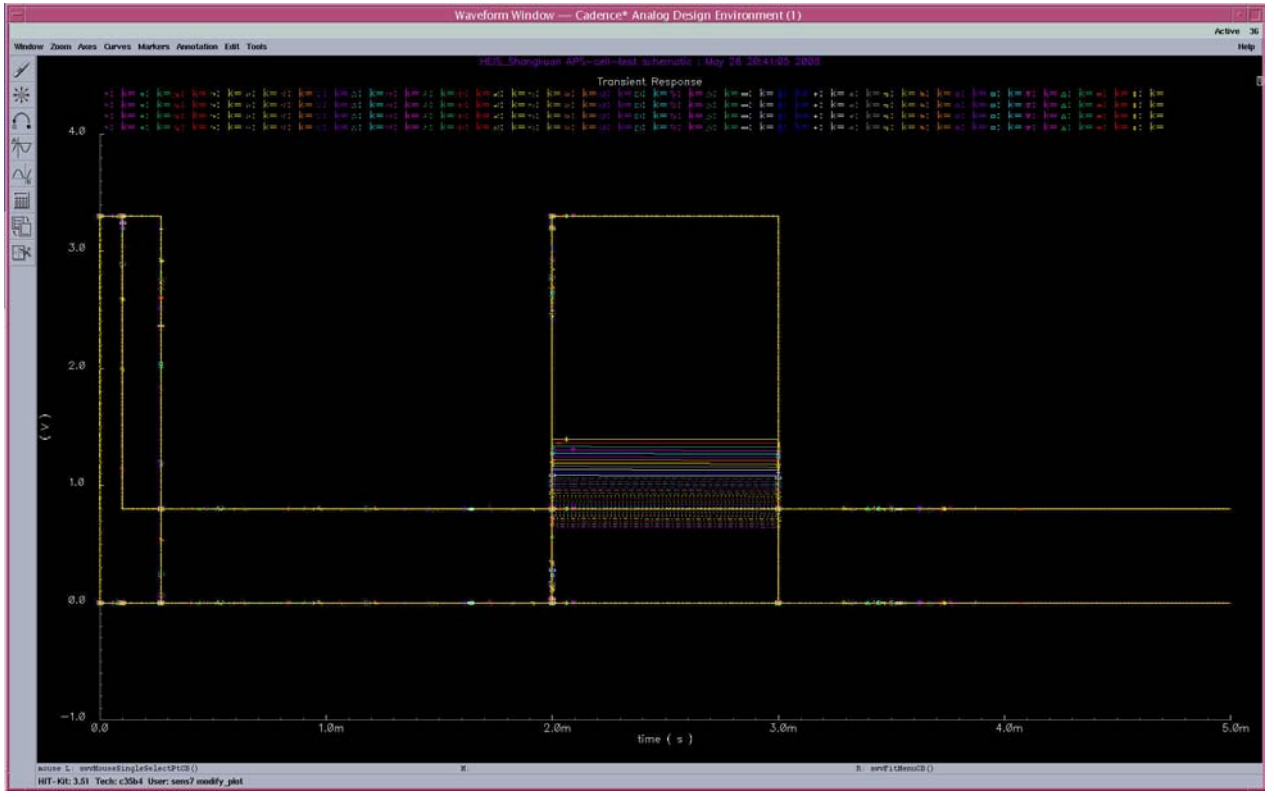
APS Row Sensor Design

Single APS Cell Simulation-Readout Time



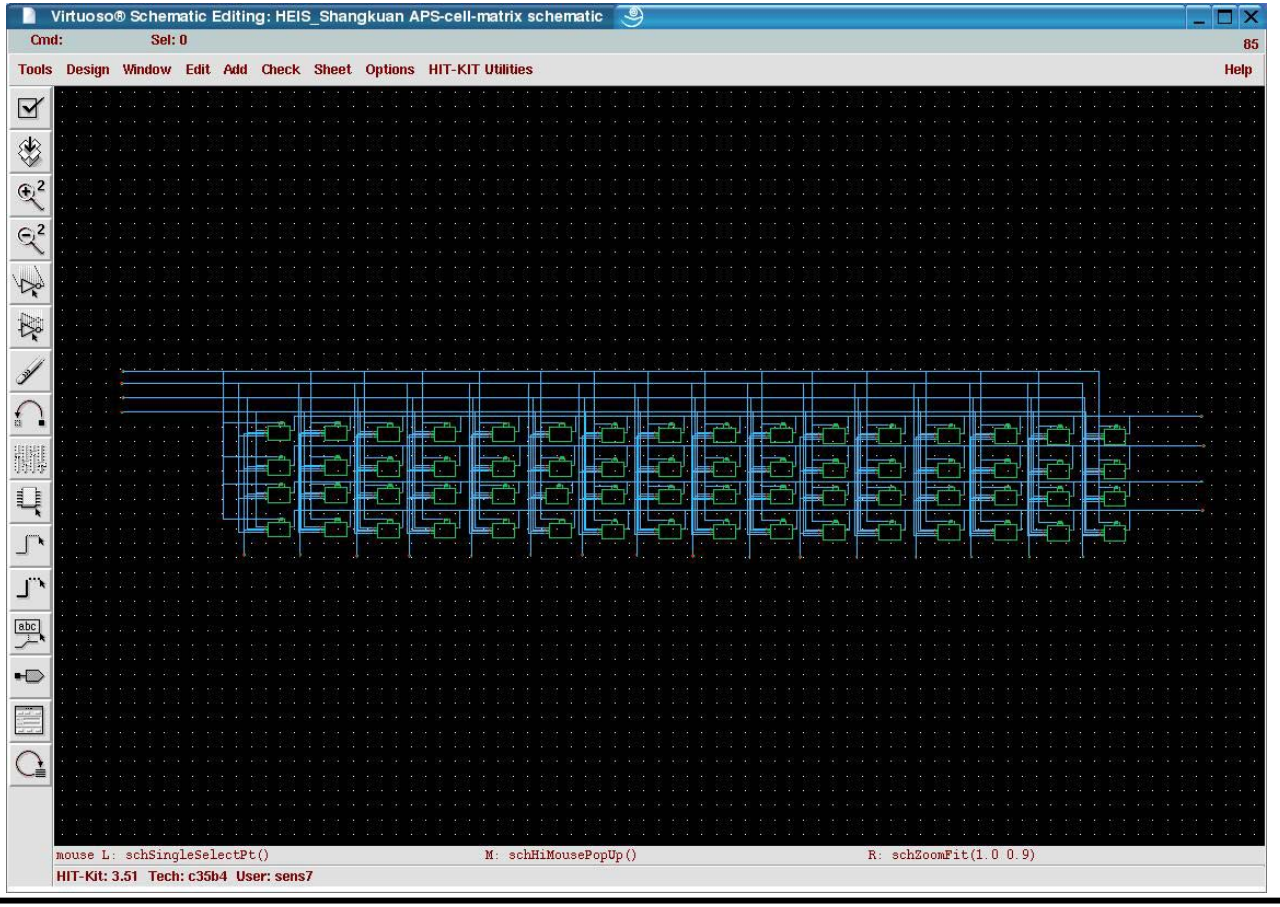
APS Row Sensor Design

APS Array Test Simulation



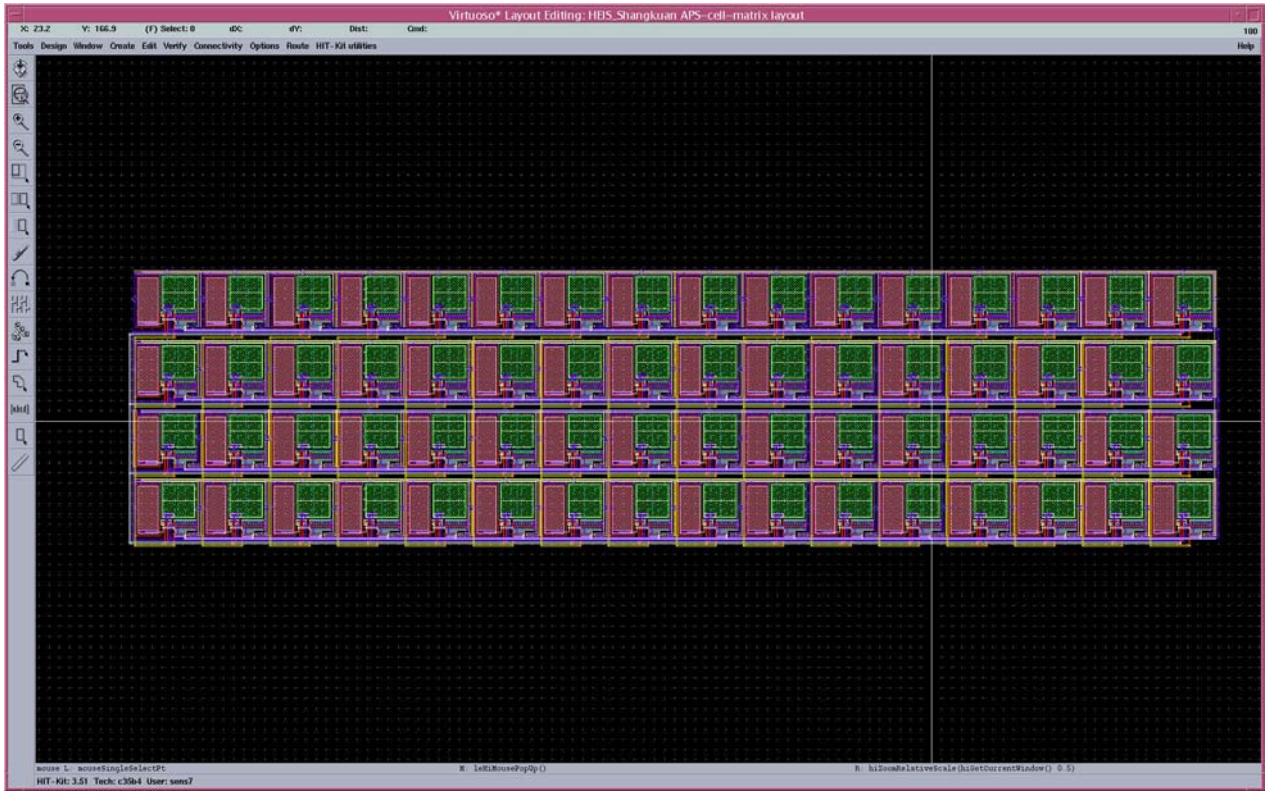
APS Row Sensor Design

APS Array Schematic



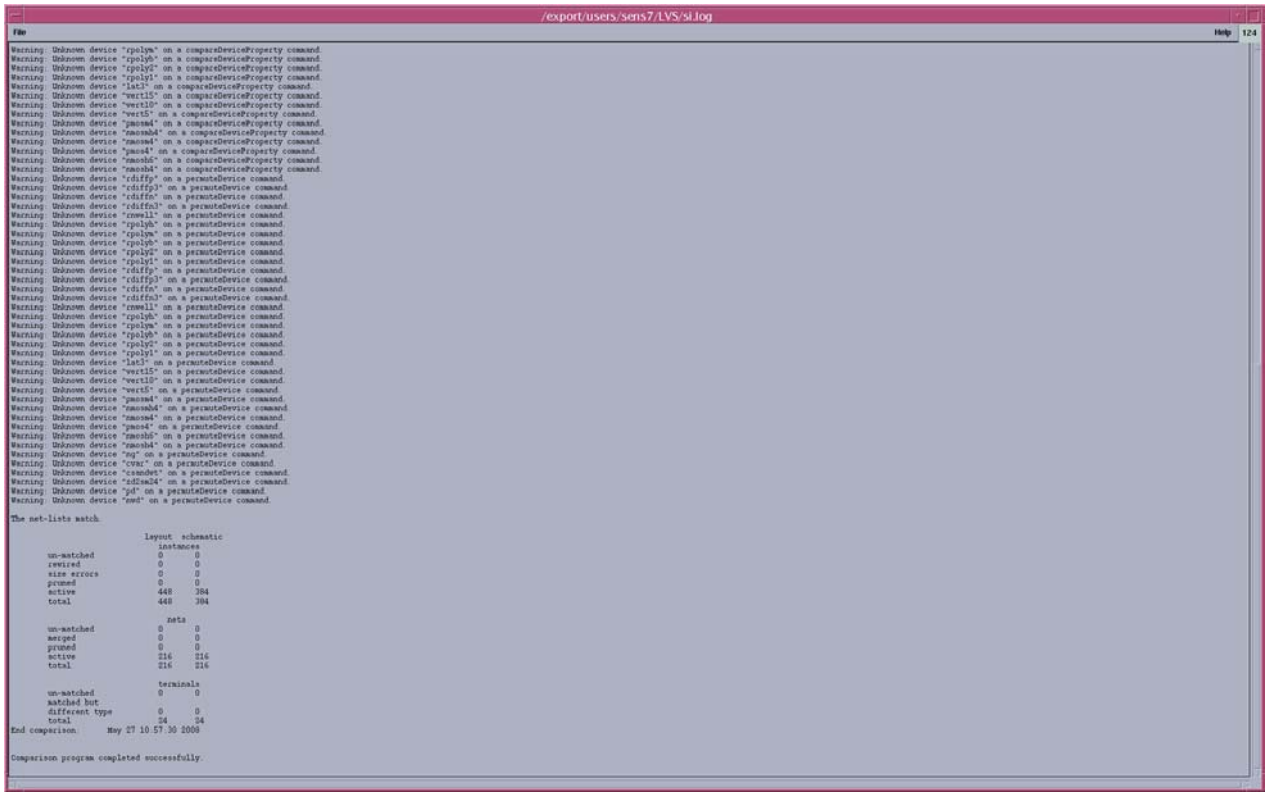
APS Row Sensor Design

APS Array Layout



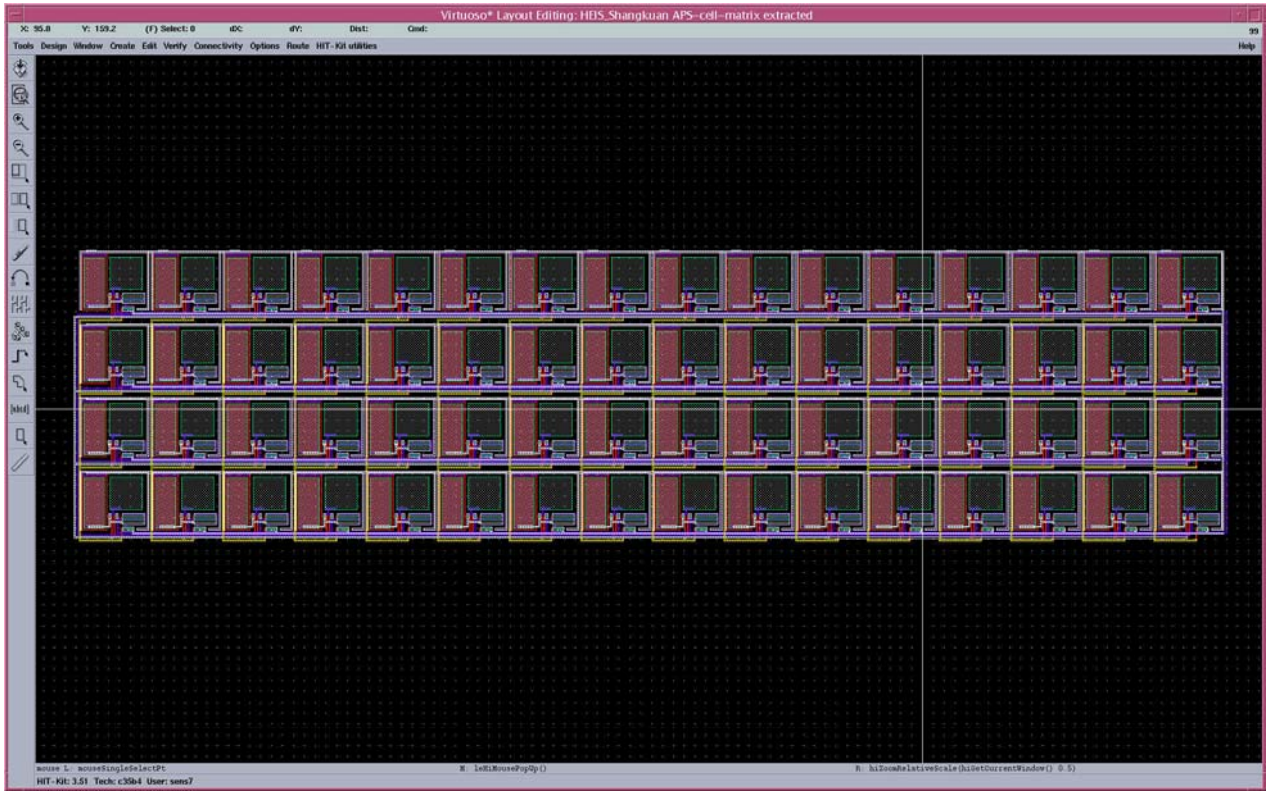
APS Row Sensor Design

APS Array LVS Check



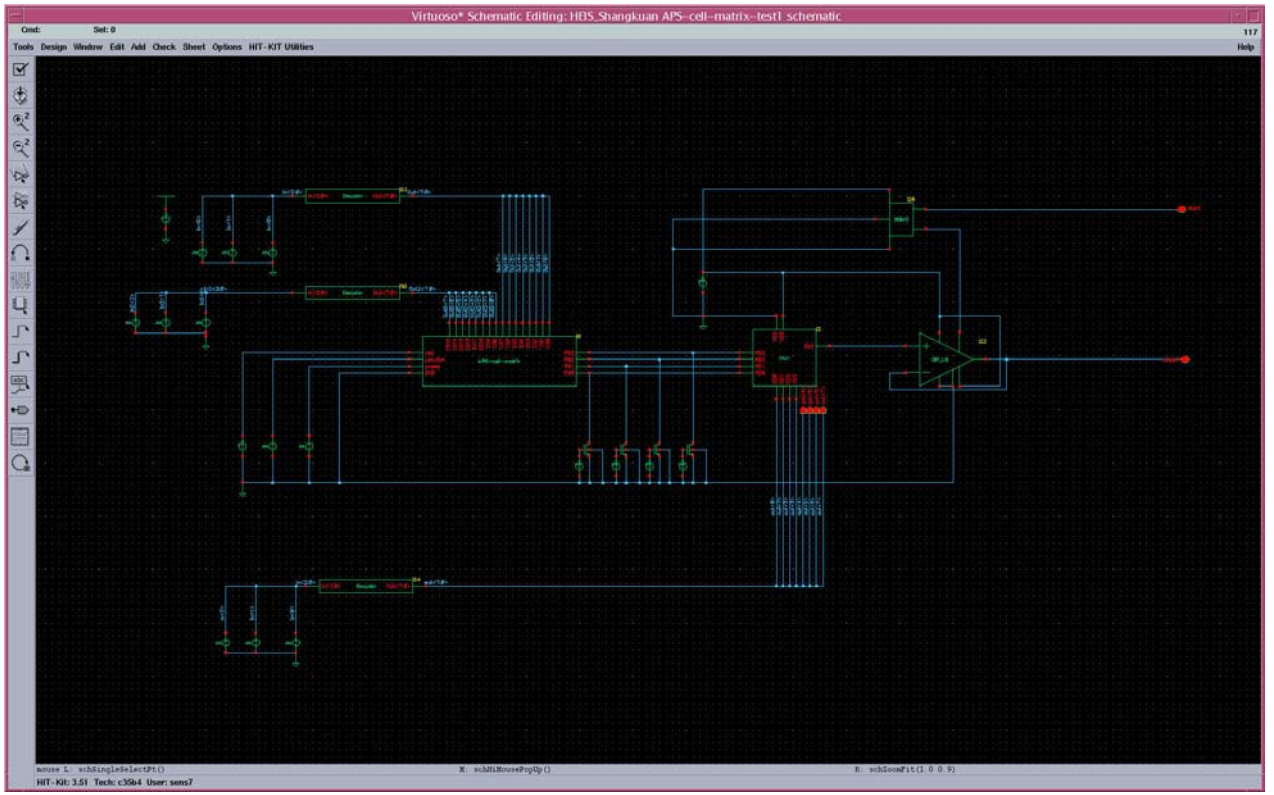
APS Row Sensor Design

APS Array Analog-Extracted



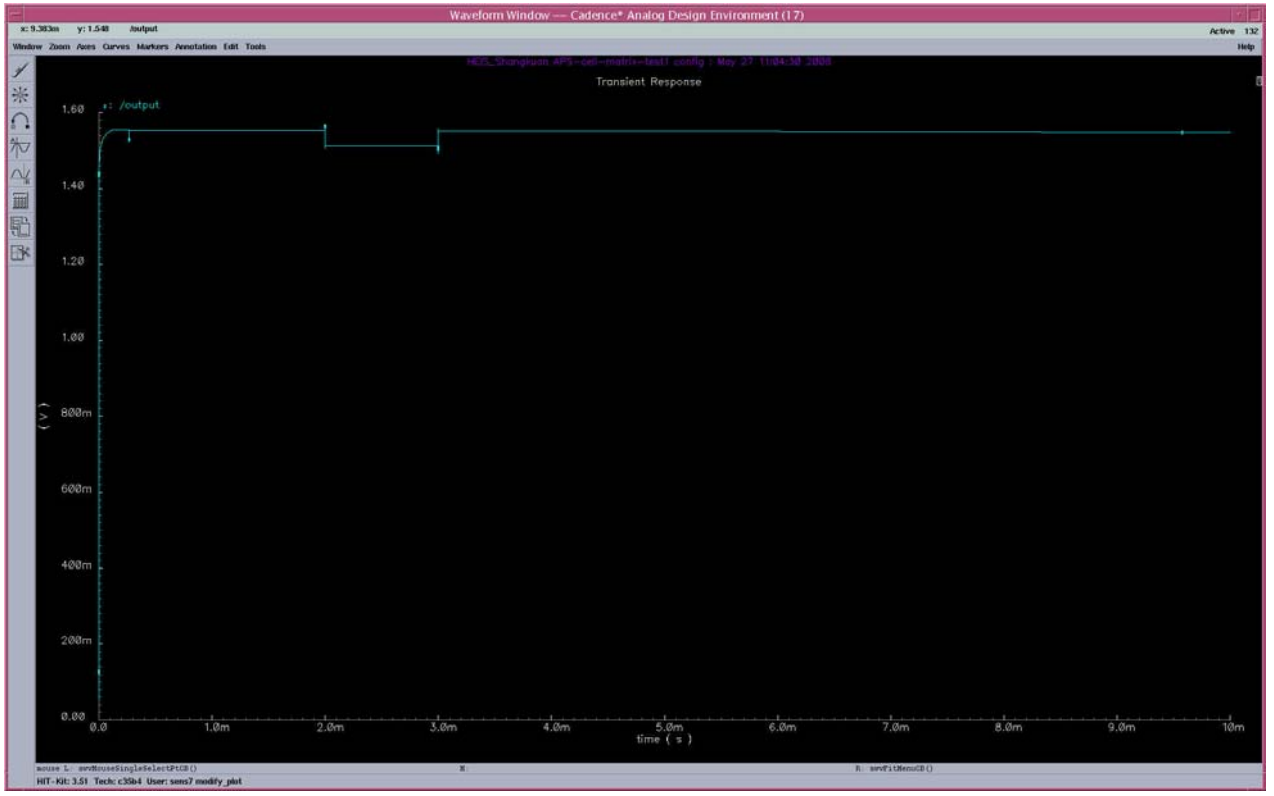
APS Row Sensor Design

APS Array Test Schematic



APS Row Sensor Design

APS Array Simulation



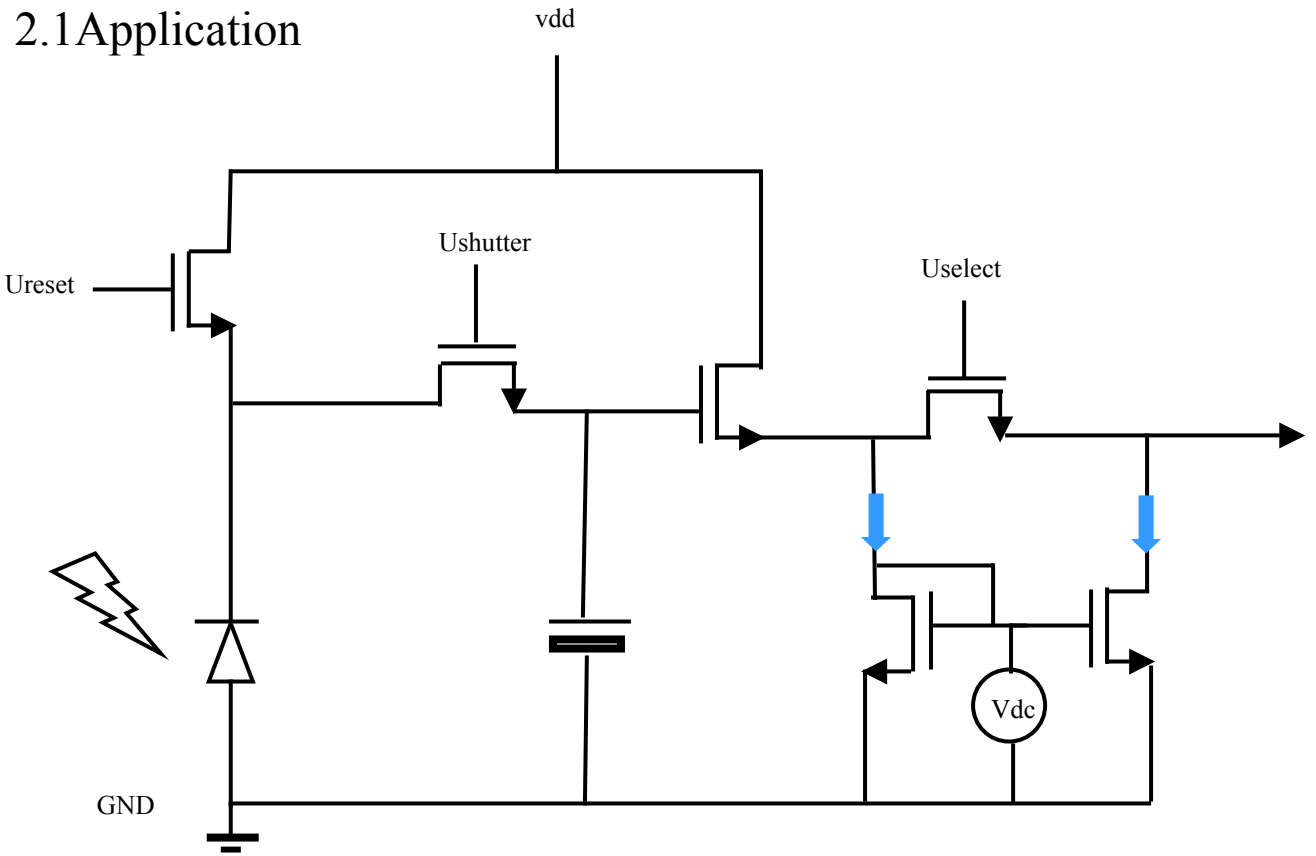
APS Row Sensor Design

1.3 Results

Technology	0.35um-4-metal COMS	Quantum Efficiency	--
Die Size	535.1uM*134.3uM	Conversion Gain	0.818uV/e
Array Size	4*16	Sensitivity	0.043/100pA
Number of Transistor	256	Dynamic Range	--
Pixel Size	32.7uM*32.3uM	Output Voltage	1.166v (I_{photo} =500pA)
Photo Detector Type	N-diffusion photodiode	Readout Time	62.5nS (I_{photo} =500pA)
Number of Transistor/Pixel	4	Bias Current	51.47uA
Fill Factor	21.3%		

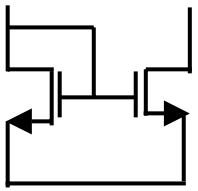
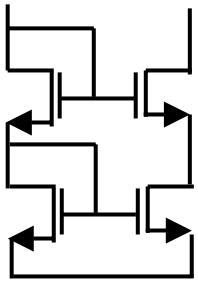
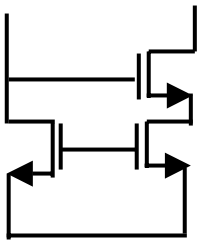
Biasing Current Circuit Design

2.1Application



Biasing Current Circuit Design

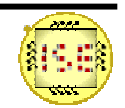
2.2 Formulas

MOS Current Mirror	Accuracy ($I_{in}=I_{out}$)	R_{out}	Aspect Ratio Calculation
	Poor	$1/\lambda I_{OUT}$	
	Good	$g_m r_o^2$	$\frac{I_{out}}{I_{in}} = \frac{(W/L)_2(1+\lambda V_{DS2})}{(W/L)_1(1+\lambda V_{DS1})}$
	Not Good	$g_m r_o^2 / 2$	

Biasing Current Circuit Design

2.3 Design Parameter

No. of Project	Dimension of Load TX (W/L Ratio)	Type of load Transistor	No. of Load Transistor	Drain Current
Project 1	1/1	NMOS	16	2.343uA
Project 2	23/1	PMOS	16	-43.0477uA
Project 3				
Project4	23/1	NMOS	16	157.481uA
Project5	1/2	NMOS	16	3.19uA
Project6	15/1	NMOS	4	51.47uA
Project8	--	--	--	11.7uA

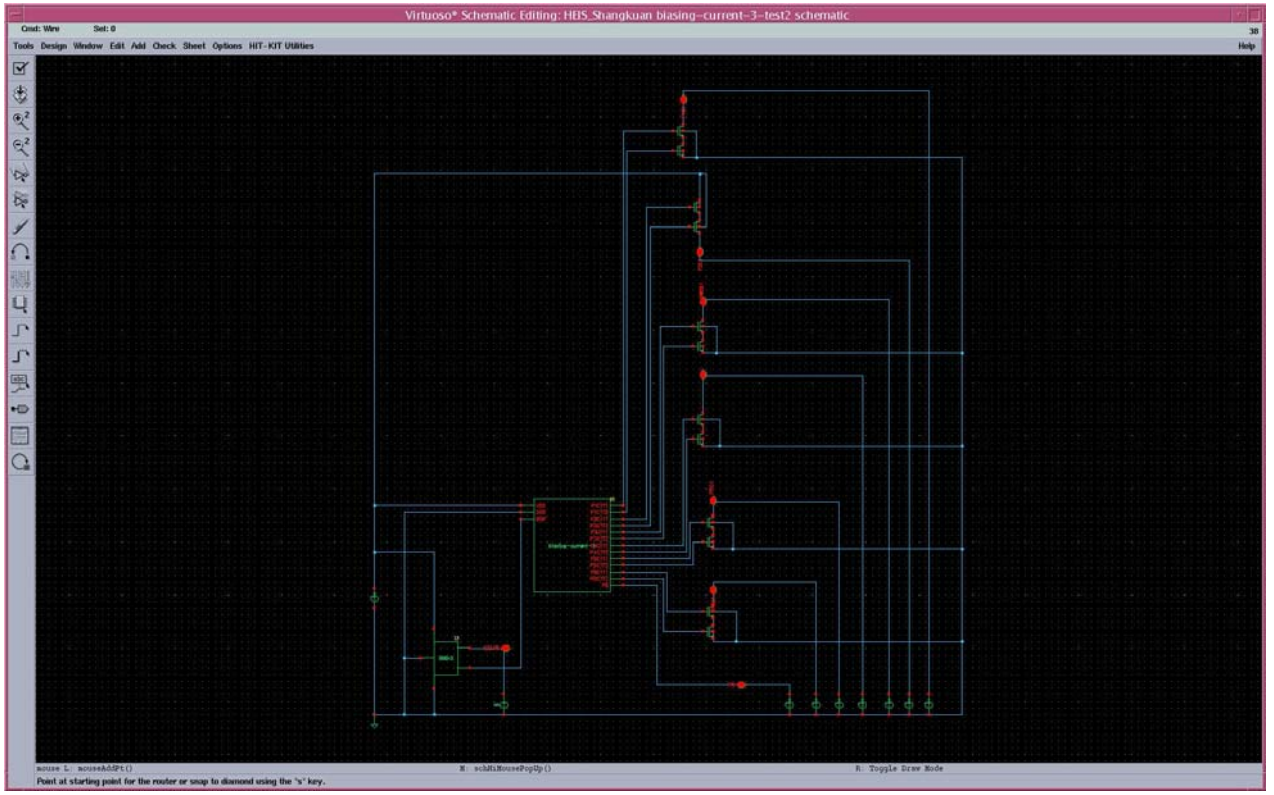


Biasing Current Circuit Design

2.4.1 Raw Schematic

Biasing Current Circuit Design

2.4.2 Raw Symbol Test



The End